What is claimed is:

1. A method for forming solder areas on electrical contacts of a device, said method comprising the steps of:

depositing a photoresist layer on a surface of said device containing said contacts;

forming respective holes in the photoresist layer to said contacts;

applying a solder layer on top of the photoresist layer and in the holes to form solder areas in the holes which contact with said contacts; and,

removing the solder layer on top of the photoresist layer and the photoresist layer using a liftoff process while leaving the solder areas on the contacts.

2. The method of claim 1, wherein the liftoff process is a tape liftoff process.

3. The method of claim 2, wherein the liftoff process comprises applying an adhesive tape overtop of the solder layer on top of the photoresist layer, and stripping away said tape to remove the solder layer and the photoresist layer while leaving said solder areas.

4. The method of claim 1, wherein the solder areas are reflowed to form solder ball contacts.

5. The method of claim 1, wherein said device is an integrated circuit wafer and the surface is the surface of said wafer.

6. The method of claim 1, wherein said device is an integrated circuit and the surface is the surface of said integrated circuit.

7. The method of claim 1, wherein said device is a circuit board and the surface is the surface of said circuit board.

8. The method of claim 1, wherein said device is a module substrate and the surface is the surface of said module substrate.

9. A process for forming a solder area on a semiconductor device comprising the steps of:

depositing a first insulating layer on at least one metal contact on a surface of said semiconductor device;

forming at least one first hole in the first insulating layer so that the at least one metal contact is exposed;

depositing metal in said at least one first hole and on top of the insulating layer to from at least one metal pad on the surface of the insulating layer;

depositing a second insulating layer over said device including over said at least one metal pad;

depositing a photoresist layer over said second insulating layer;

forming at least one second hole in the second insulating layer and the photoresist layer to expose said at least one metal pad;

applying a solder layer over the photoresist layer and in the at least one second hole to from at least one solder area in the second hole which is in contact with said at least one metal pad; and,

removing the photoresist layer and solder layer from the device using a liftoff process while leaving the solder area in contact with said at least one metal pad.

10. The process of claim 9, wherein the liftoff process is a tape liftoff process.

11. The process of claim 9, wherein the second insulating layer is polyimide.

12. The process of claim 9, wherein the first insulating layer is silicon dioxide.

13. The process of claim 9, wherein the photoresist layer is at least 2 microns thick.

14. The process of claim 9, wherein the first insulating layer is planarized before the at least one first hole is formed.

15. The process of claim 9, wherein the metal pad comprises a metal stack comprising four different metal levels.

16. The process of claim 15, wherein the metal levels comprise Zirconium, Nickel, Copper and Gold.

17. The process of claim 9, wherein said photoresist layer comprises a thin layer of silicon nitride interposed between an upper layer and a lower layer of photoresist.

18. The process of claim 9, wherein the first insulating layer is polished by chemical mechanical polishing before the at least one first hole is formed.

19. The process of claim 9, wherein the at least one first hole is formed in the first insulating layer by a photoresist etch process.

20. The process of claim 9, wherein at least one portion of the second insulating layer is removed prior to the application of the solder layer.

21. The process of claim 20, wherein the at least one second hole is formed in the photoresist layer above the area in the second insulating layer which has been removed.

22. The process of claim 9, wherein the first insulating layer is at least 2 microns thicker than the at least one metal contact.

23. The process of claim 16, wherein the Zirconium layer is at least 500 Angstroms thick.

24. The process of claim 16, wherein the Nickel layer is at least 750 Angstroms thick.

25. The process of claim 16, wherein the Copper layer is at least 5000 Angstroms thick.

26. The process of claim 16, wherein the Gold layer is at least 750 Angstroms thick.

27. The process of claim 17, wherein the silicon nitride layer is at least 500 Angstroms thick, and the upper and lower layers of photoresist are at least .5 microns thick.

28. The process of claim 9, wherein the solder layer applied is at least 2.33 microns thick.

29. The process of claim 9, wherein the solder area has a diameter less than 100 microns.

30. The process of claim 9, wherein the solder area has a diameter less than 50 microns.

31. The process of claim 9, wherein the solder area has a diameter less than 25 microns.

32. The process of claim 9, wherein the solder area has a diameter less than 10 microns.

33. The process of claim 9, wherein the solder area has a diameter approximately 2 microns.

34. The process of claim 9, wherein the solder area is reflowed to form a solder contact.

35. The process of claim 9, wherein said semiconductor device is an integrated circuit wafer.

36. The process of claim 9, wherein said semiconductor device is an integrated circuit.

37. A method for forming a solder area on a semiconductor device comprising the steps of:

depositing an insulating layer over at least one metal pad formed on the semiconductor device;

depositing a photoresist layer over said insulating layer;

forming at least one hole in the insulating layer and the photoresist layer to expose said at least one metal pad;

applying a solder layer over the photoresist layer and in the at least one hole to from at least one solder area in the hole; and,

removing the photoresist layer and solder layer using a liftoff process while leaving the solder area on the metal pad.

38. The method of claim 37, where the liftoff process is a tape liftoff process.

39. The method of claim 37, wherein the liftoff process comprises applying an adhesive tape overtop of the solder layer, and stripping away said tape to remove the solder layer and the photoresist layer while leaving said solder area.

40. A semiconductor device comprising:

a semiconductor structure having at least one metal contact formed on a surface thereof;

a first insulator layer overlying said at least one metal contact;

at least one metal pad overlying said first insulator layer and in contact with said at least one metal contact;

a second insulator layer overlying said at least one metal pad; and,

at least one solder contact formed in the second insulator and in contact with said at least one metal pad, said solder contact having a diameter less than 100 microns.

41. The semiconductor device of claim 40, wherein the solder contacts have a diameter less than 50 microns.

42. The semiconductor device of claim 40, wherein the solder contacts have a diameter less than 25 microns.

43. The semiconductor device of claim 40, wherein the solder contacts have a diameter less than 10 microns.

44. The semiconductor device of claim 40, wherein the solder contacts have a diameter of approximately 2 microns.

45. The semiconductor device of claim 40, wherein said at least one metal contact is connected to said at least one metal pad by a via hole formed in the first insulator.

46. The semiconductor device of claim 40, wherein the at least one solder contact extends from a top surface of the second insulator to the metal pad by a through hole formed in the second insulator.

47. The semiconductor device of claim 40, wherein the at least one metal pad lies at least partially overtop of the at least one metal contact.

48. The semiconductor device of claim 40, wherein the semiconductor device is an integrated circuit chip.

49. The semiconductor device of claim 40, wherein the semiconductor device is an integrated circuit wafer.

50. The semiconductor device of claim 40, wherein the semiconductor device is bonded to a module substrate.

51. The semiconductor device of claim 40, wherein the semiconductor device is bonded to a circuit board.

52. A method for forming solder areas on electrical contacts present at a surface of an electrical device, said method comprising the steps of:

depositing a liftoff layer on said surface;

forming respective holes in the liftoff layer to expose said contacts;

applying a solder layer on top of the liftoff layer and in the holes to form solder areas in the holes which are in contact with respective ones of said electrical contacts; and,

removing the solder layer and liftoff layer using a liftoff process while leaving the solder areas.

53. The method of claim 52, wherein the liftoff process comprises applying an adhesive tape overtop of the solder layer, and stripping away said tape to remove the solder layer and the liftoff layer while leaving said solder areas.

54. The method of claim 52, wherein the liftoff layer comprises an insulating layer.

55. The method of claim 54, wherein the insulating layer is a polyimide layer which can be peeled away.

56. The method of claim 52, wherein the liftoff process is a tape liftoff process.

57. The method of claim 52, wherein the electrical device is an integrated circuit chip.

58. The method of claim 52, wherein the electrical device is an integrated circuit wafer.

59. The method of claim 52, wherein the electrical device is a circuit board.

60. The method of claim 52, wherein the electrical device is a module substrate.

61. The method of claim 52, wherein the liftoff layer is photoresist layer.

62. A method of forming contact pads and solder areas on an electrical device comprising the steps of:

depositing a photoresist layer on the surface of an electrical device containing vias;

forming respective holes in the photoresist aligned with said vias;

applying a layer of contact metal to form contacts in the vias and in the holes overlying said vias;

applying a layer of solder to form solder areas on top of the contacts in the holes over said vias;

removing the solder and the contact metal which lies on top of the photoresist layer using a liftoff process, while leaving the solder areas and contacts which lie overtop of the vias.

63. The method of claim 62, wherein the liftoff process is a tape liftoff process.

64. The method of claim 62, wherein the solder areas and contacts are reflowed to form solder ball contacts.

65. The method of claim 62, wherein the electrical device is an integrated circuit.

66. The method of claim 62, wherein the electrical device is a circuit board.

67. The method of claim 62, wherein the electrical device is a module substrate.

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